PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H02H 7/122

A1

(11) International Publication Number: WO 97/14205

(43) International Publication Date: 17 April 1997 (17.04.97)

(21) International Application Number: PCT/DK96/00418

(22) International Filing Date: 3 October 1996 (03.10.96)

(30) Priority Data:
1118/95 6 October 1995 (06.10.95) DK

(71) Applicant (*for all designated States except US*): DANFOSS A/S [DK/DK]; DK-6430 Nordborg (DK).

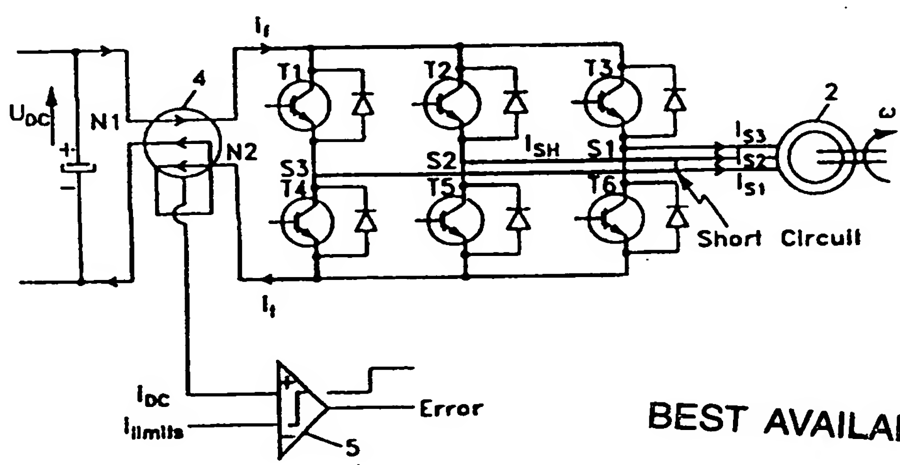
(72) Inventor; and
(75) Inventor/Applicant (*for US only*): BLÅBJERG, Frede [DK/DK]; Forårsvej 78 B, DK-9270 Aalborg ø (DK).

(74) Comm n Representative: DANFOSS A/S; Patent Dept., DK-6430 Nordborg (DK).

(81) Designated States: AM, AT, AU, BA, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KR, KZ, LT, LU, LV, MD, MK, MX, NO, NZ, PL, PT, RO, RU, SE, SG, SI, SK, TR, UA, US, UZ, VN, Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: METHOD FOR MEASURING FAULT CURRENTS IN AN INVERTER AND INVERTER WITH CONTROLLED SEMICONDUCTOR SWITCHES



(57) Abstract

When measuring fault currents in an inverter, in which controlled semiconductor switches are pulse width modulated, PWM-VSI, to convert a DC voltage from an intermediary circuit to a 3-phase AC v ltage, DC currents are measured in the positive and the negative rail of the inverter, s that it is possible to detect faults originating from both short-circuits and earthing faults, maintaining a high sensitivity when reconstructing phase currents, which can be made by a so-called vector modulation, called (SFAVM), in which the states of the individual transistor switches are defined in a vector room (SFAVM) having six active states in which current fl ws in the inverter and two active states in which no current flows in the inverter. On the basis of the DC current measurements the phase currents can be reconstructed, and all faults can be detected. As mentioned, the measurement takes place as a measurement f DC currents, and for this purpose two transducers are used, which are constructed in a way that at the same current they give two different physical values, so that if there is no fault n the inverter, the phase current can still be reconstructed. The invention is especially expedient in connection with motor controls, active inverters, active filters, compensators, etc.

BEST AVAILABLE COPY

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia
AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CS	Czechoslovakia
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgystan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakhstan
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam

Method for measuring fault currents in an inverter and inverter with controlled semiconductor switches

The invention concerns a method for measuring fault currents in an inverter, in which controlled semiconductor switches are pulse width modulated, hereby converting a DC voltage from an intermediary circuit to a multi-phase AC voltage, and where phase currents are reconstructed by measuring a current in the intermediary circuit, and current fault detection is made by measuring both the forward current flowing to the switches and the reverse current flowing from the switches.

The invention also concerns an inverter with controlled semiconductor switches, which are pulse width modulated, hereby converting a DC voltage from an intermediary circuit to a multi-phase AC voltage, and where phase currents are reconstructed by a measuring device measuring a current in the intermediary circuit, and where the measuring device, through measurements of the forward current flowing to the semiconductor switches and the reverse current flowing from the switches, is also acting as fault current detector.

In an article published by the Institute of Energy Techniques, Alborg University, by Frede Blaabjerg and John Pedersen with the title "A new low-cost, fully fault protected PWM-VSI inverter with true phase-current information" a method of the sort mentioned above is described. The article was published by IPEC '95, Yokohama, Japan, 3 to 7 April 1995.

The inverter consists of six transistors controlled through eight possible switch states. Of these, two give no voltage between the phase-phase wires, while the remaining six generate a voltage, which, when connected to a load, leads to a voltage between the phases, which again leads to a current i_{DC} in the intermediary circuit. The current flows towards the transistors in the positive current rail of the intermediary circuit and returns from the transistors in the negative current rail of the intermediary circuit. The three phase currents can be reconstructed by measurements e.g. in the negative current rail of the intermediary circuit, as is also stated in the article. This will also be dealt with later.

E.g. the inverter is used for motor controls, but it can also be used in active inverters, active filters, compensators etc.

It is extremely important that faults, e.g. short circuits in the inverter are discovered quickly, as considerable amperages are involved.

In the article various fault detections are shown. In a first embodiment the fault currents are measured with four current sensors, one for each phase and one for the DC current. Obviously, this is an expensive solution, and in the article it is therefore proposed to use the DC current measurements partly for reconstructing the three phase currents, partly for fault detection, though an additional current sensor capable of sensing earthing faults is used around the phases.

Finally, the article mentions a method, for which only one current sensor is used, for reconstruction of the three phase currents, which are connected in a way that all faults can be detected. The current sensor measures the forward and

the reverse DC currents and the two currents are added in the current measurement. However, this principle has one disadvantage, namely that the current sensor measures the double current, causing that the resolutions of the measurement and the earthing fault detection are halved.

The purpose of the invention is to improve the reconstruction of the three phase currents mentioned above in a way that the resolution of both measurement and fault detection reaches an optimum.

According to the invention, this is obtained by a method as stated in the preamble of claim 1, which is characteristic in that the current measurements are made by means of a current sensor measuring the difference between the forward current and the reverse current, by which the forward current is converted to a 1st physical value, while the reverse current is converted to a 2nd physical value, the 1st and the 2nd physical values being different when the forward current and the reverse current are equal.

In this way any fault can be detected maintaining the reconstruction of the phase currents, as the sum of the two physical values will be different from zero, when the inverter is working without faults. Especially faults can be detected when the inverter is set in a state in which there is no voltage difference between the phases, while the reconstruction of the phase currents can take place on the basis of the sum values of the physical sizes.

As stated in claim 2, the forward current and the reverse current are measured by a current sensor having two transducers, of which the first one is converting the forward current to a 1st physical value, while the other converts the reverse current to the 2nd physical value.

If coils with different winding numbers are used as transducers, especially in a way that one of the coils has one winding more than the other, a maximum resolution is obtained. Besides, an optimum frequency characteristic is obtained if one of the coils has exactly one winding.

As mentioned, the invention also concerns an inverter with controlled semiconductor switches of the sort mentioned in the preamble of claim 6. This inverter is characteristic in that the measuring device converts the forward current to a 1st physical value, while the reverse current is converted to a 2nd physical value, the 1st physcial value being different from the 2nd physical value, if the forward and reverse currents are equal.

Advantageous embodiments of the invention appear from the dependent claims.

In the following the invention will be explained on the basis of the figures, in which

Fig. 1 shows a known inverter of the PWM-VSI type with a current sensor

Fig. 2 also shows a known inverter of the PWM-VSI type but with protection against fault currents

Fig. 3 uses vector notation and shows how the inverter can be modulated

Fig. 4 shows the geometrical placing of the voltage vectors of a 3-phase AC

Fig. 5 shows a table of phase currents from the inverter as a function of the voltage vectors according to fig. 3 and 4

Fig. 6 shows a current circuit with a protection principle in accordance with the invention

Fig. 7 shows an example of a short-circuiting in an inverter branch

Fig. 8 shows an example of short circuiting of two phases

Fig. 9 shows an example of an earthing fault

Fig. 10 shows the current sensor set-up for use with the protection principle according to the invention

Fig. 1 shows a three-phase PWM-VSI (pulse width modulated voltage source inverter) consisting of six transistors, T1, T2, T3, T4, T5 and T6, in a three-phase inverter bridge, each of which has a commonly known free-wheeling diode connected in parallel. At a suitable application of voltages, $u_{[illegible]}$, $u_{[illegible]}$ and $u_{[illegible]}$ on the bases/gates of the transistors, cf. later, phase voltages and phase currents, $i_{[illegible]}$, $i_{[illegible]}$ and $i_{[illegible]}$, will be produced on the outputs of the transistors connected in pairs, which phase voltages and phase currents can be lead to a load in the form of a motor as control current.

The transistors are supplied with a DC voltage from an intermediary current circuit 1. At a suitable conversion of the transistors from conducting to non-conducting state, the inverter bridge converts the AC voltage to a three-phase AC voltage.

BEST AVAILABLE COPY

In a known way the phase currents can be reconstructed by measuring the current i_{DC} in the intermediary circuit. Further a measuring of i_{DC} can disclose if there are faults in the inverter, for instance if a current, i_{DC}, is measured, even if voltages are applied for the bases/gate of the transistors, which should make the intermediary circuit currentless. However, the disclosure of the fault is not certain in all cases with the circuit shown in fig. 1, for instance if all the transistors T1, T2 and T3 are on, and there is an earthing fault occurring in the load, and thus not reaching the current sensor. Analogue considerations

apply for the transistors T4, T5 and T6, if the current sensor is placed in the current rail in the intermediary current circuit carrying the forward current.

Fig. 2 shows an inverter which is different from the one shown in fig. 1 in that in the intermediary current circuit both a forward current and a reverse current are measured, which are then added. In this way also earthing faults can be discovered, if all three transistors T1, T2 and T3 are on. However, the disadvantage of this is that the distribution of the current measured halves the resolution of the determination of the phase currents, and also of the earthing fault detection.

In connection with fig. 3 to 5, the following will be an explanation of how the inverter is controlled in accordance with the invention.

The transistors T1, T2, T3, T4, T5 and T6 are switched in a way that uniquely defined currents occur in the intermediary circuit, which for every single switch state can be referred to a certain phase, cf. fig. 5, i.e. the currents $i_{[illegible]}$, $-i_{[illegible]}$, $i_{[illegible]}$, $-i_{[illegible]}$, $i_{[illegible]}$, $-i_{[illegible]}$. Further, the inverter can be currentless in the intermediary circuit. Symbolically, this can be expressed by a vector notation, which is shown in the table in fig. 5. As appears from this table, a vector of the form (x, y, z) has been allocated to each of the eight switch states, in which x expresses the state of transistor T1, in a way that logical "1" means on, while logical "0" means off. The same applies for transistor T2, the state of which is y, and transistor T3 with the state z. Please also note that the transistors T4, T5 and T6 are working complementarily with the transistors T1, T2 and T3, meaning that when T1 is on, T4 is off and vice versa, etc.

As shown in fig. 3, the application on the phases of the voltage vector (100) for the period T1, and the voltage vector (110) for the period T2, corresponding to a pulse width modulation, enables the realisation of a customized voltage, u_s, with a desired frequency and amplitude on a load. The angle of u_s is directly proportional to the relative duration of the periods. Please note that when (x, y, z) = (0, 0, 0) or (1, 1, 1), the load is disconnected from the intermediary circuit, i.e. $u_s = 0$.

As can also be seen from fig. 4 when compared with fig. 5, any voltage can be applied with a load at a suitable selection of (x, y, z).

Fig. 4 shows a symbolic vector diagram divided into 6 sectors marked I, II, III, IV, V and VI. Each of these sectors is defined by the voltage vectors from the table in fig. 5, so that a given phase current can be fed to a load.

An example of the application of a voltage vector u in sector IV, corresponding to the phase currents i_{s1} and $-i_{s3}$, could be the switching of the transistors in the following vector sequence:

(000), (010), (011), (111), (111), (011), (010), (000).

Please note that the last phase current is determined on the basis of the equation:

$$i_{s1} + i_{s2} + i_{s3} = 0$$

When changing the switching frequency, and the duration of the individual phase currents, a given voltage vector can thus be produced for a load with the switching sequence in sector IV mentioned above.

BEST AVAILABLE COPY

In a completely analogue way the voltage vectors in the other sectors can be produced.

As a modulation of the inverter will produce voltage vectors by switching between the eight states in fig. 5, it is obvious that measuring i will enable the determination of the three-phase currents, as there is a unique correlation between the phase currents and i.

The following is an explanation of how a measuring of i in accordance with the invention can improve the detection of possible faults in the inverter. The principle is shown in fig. 6, showing, like fig. 1 and 2, a three phase inverter connected to a load in the form of a three-phase AC motor.

As can be seen from the figure, the current measuring is made, like in fig. 2, by measuring both the forward and the reverse i currents. The difference is that the measuring is made so that the forward i current can be distinguished from the reverse i current.

To be explicit, the following applies:

$$i = N1 \times i - N2 \times i,$$

where N1 and N2 are the numbers of windings on a coil in a current sensor.

If N1 = N2 when there are no earthing or phase-zero faults, the two currents will neutralise each other and give the resulting $i = 0$, and though this ensures that the inverter is faultless, it also makes the information needed for the reconstruction of phase currents disappear.

If, however, N1 = N2, a resulting $i_{[illegible]}$ current can be measured for reconstructing the phase current under preservation of fault detection in both the positive and the negative DC branch, and, that is, also preserving the high sensitivity.

In other words, compared with the set-up according to fig. 1, full protection of the inverter in the DC intermediary circuit is obtained, also when the voltage vector is applied with (000) or (111), where the phases are disconnected from one of the current rails of the intermediary circuit, and compared with the embodiment in fig. 2 a high resolution under preservation of full fault detection is ensured.

In this connection it must also be noted that in relation to the embodiment according to fig. 2, the driving area of the current sensor can be halved from e.g. 50 A to 25 A, so that it becomes cheaper.

Out of regard for the dynamic range with regard to frequency, it is preferred that N1 and N2 have as few windings as possible. At the same time this ensures the lowest possible demands on overvoltage protection of the power switches.

For example, N1 = N2 + 1, at N2 = 1.

In the following some possible fault situations in a three phase inverter will be described in connection with fig. 7 to 9.

Fig. 7 shows a short-circuiting of an inverter branch, marked with a bold line, i.e. T1 and T4 are on at the same time. The current $i_{[illegible]}$ will run in the short-circuited branch, where $i_{[illegible]} = i_{[illegible]} = i_{[illegible]}$. At a comparison in a comparator 5, in which a limit value $I_{[illegible]}$ is compared with $i_{[illegible]}$, the fault can

be detected. Of course, the same applies for the other inverter branches.

Fig. 8 shows a fault situation, in which two phases are short-circuited. The applied voltage vector is (011).

In this case i_{SH} will be able to run as shown with a bold line, i.e. from T2 through the phases i_{S2} and i_{S3} and through T4. Like in the fault situation in fig. 7, the current i_2 = i_3 = i_{SH} can be compared with a limit value in a comparator, and give fault message.

Finally, fig. 9 shows a fault situation, in which an earthing fault has occurred, here shown with a bold line, said fault being caused by an unintentional earthing of one of the phases S3.

In this situation there are two possibilities, namely a so-called small earthing fault and a proper short-circuiting to earth.

A small earthing fault is detected by applying one of the voltage vectors (000) or (111) to the phases, and if a comparator circuit 5 finds that $I_{[illegible]}$ is higher than $I_{[illegible]}$, the earthing fault will be detected in the AND-circuit 7, which only permits passage, when one of the voltage vectors (000) or (111) is applied.

A proper short-circuiting to earth is detected as described earlier through a comparison of $i_{[illegible]}$ and I_{limit} in the comparator 5.

Faults for a possible 0-conductor can be detected in the same way.

Fig. 10 is a schematic view of the current measurements in an embodiment. As shown in the figure, a differential transformer 9 with two coils 10, 11, has been inserted between the inverter 12 and the intermediary circuit 1, the forward current i_f being connected to the coil 10, while the reverse current i_r is connected to the coil 11. A Hall element 13 is placed in the slot of the differential transformer. The Hall element converts the magnetic field built up in the slot to a current taken out through an amplifier 14.

The mode of operation is as follows:

If the forward current i_f has the same numerical value as the reverse current i_r, a magnetic field will be built up in the slot of the transformer when the coils 10 and 11 have different winding numbers, for instance as suggested in the figure, in which coil 10 has two windings, while the coil 11 has three windings. This magnetic field can then be detected by the Hall element, which converts the magnetic field to a current.

With this measuring set-up the current measuring can be used for both fault detection and reconstruction of the phase currents.

Even though the invention is described in connection with an inverter connected to a motor, nothing prevents the use of the principles of the invention in other connections, within the frames stated by the patent claims, for instance with active inverters, active filters, compensators etc.

Patent Claims

1. Method for measuring fault currents in an inverter (12), in which controlled semiconductor switches (T1, T2, T3, T4, T5, T6) are pulse width modulated, hereby converting a DC voltage from an intermediary circuit (1) to a multi-phase AC voltage, where phase currents are reconstructed by measuring a current in the intermediary circuit, and where current fault detection is made by measuring both the forward current flowing to the switches and the reverse current flowing from the switches, **characterised in that** the current measurements are made by means of a current sensor (4) measuring the difference between the forward current and the reverse current, by which the forward current is converted to a 1st physical value and the reverse current is converted to a 2nd physical value, the 1st and the 2nd physical value being different when the forward current and the reverse current are equal.

2. Method according to claim 1, **characterised in that** the forward current and the reverse current are measured by a current sensor (4) having two transducers (10, 11), of which the first transducer (10) is converting the forward current to the 1st physical value, while the second transducer (11) is converting the reverse current to the 2nd physical value.

3. Method according to claim 2, **characterised in that** two coils (10, 11) with different winding numbers are used as transducers.

4. Method according to claim 3, **characterised in that** the winding number of one of the coils (11) is one higher than the winding number of the other coil (10).

5. Method according to claim 3 or 4, **characterised in that** one of the coils has exactly one winding.

6. Inverter (12) with controlled semiconductor switches (T1, T2, T3, T4, T5, T6), which are pulse width modulated, hereby converting a DC voltage from an intermediary circuit (1) to a multi-phase AC voltage, where phase currents are reconstructed by a measuring device (4) measuring a current in the intermediary circuit, and where the measuring device, through measurements of the forward current flowing to the semiconductor switches and the reverse current flowing from the switches, is also acting as fault current detector, **characterised in that** the measuring device (4) is converting the forward current to a 1st physical value, while the reverse current is converted to a 2nd physical value, the 1st and the 2nd physical value being different when the forward current and the reverse current are equal.

7. Inverter according to claim 6, **characterised in that** the measuring device (4) includes two transducers (10, 11) for conversion of the forward and reverse currents to the 1st and the 2nd physical value, respectively.

8. Inverter according to claim 7, **characterised in that** the measuring device is a differential transformer (9) with two windings.

9. Inverter according to claim 8, **characterised in that** the differential transformer (9) is connected to a Hall-element (13).

10. Inverter according to claim 8 or 9, **characterised in that** the differential transformer (9) has two windings with different winding numbers.

11. Inverter according to claim 10, **characterised in that** one of the coils (11) has one winding more than the other coil (10).

12. Inverter according to claim 10 or 11, **characterised in that** one of the coils has exactly one winding.

13. Inverter according to any of the claims 6 to 11, **characterised in that** the fault current detector (4) is made for fault detection of a short-circuiting in an inverter branch.

14. Inverter according to any of the claims 6 to 11, **characterised in that** the fault current detector (4) is made for fault detection of a short-circuiting of two phases.

15. Inverter according to any of the claims 6 to 11, **characterised in that** the fault current detector (4) is made for fault detection of a short-circuiting to earth.

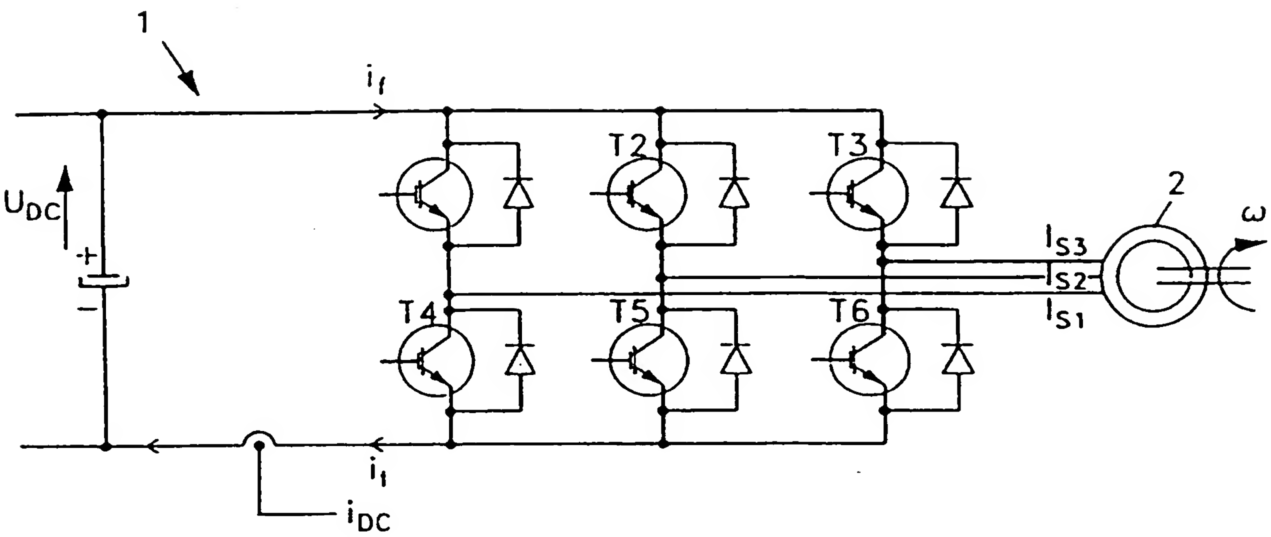


Fig. 1

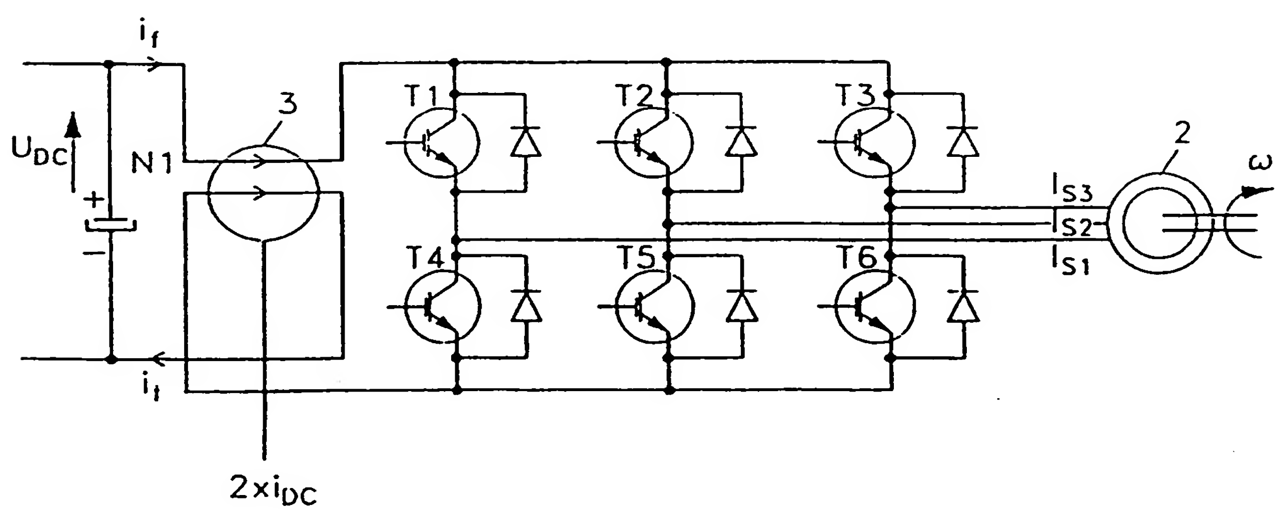


Fig. 2

BEST AVAILABLE COPY

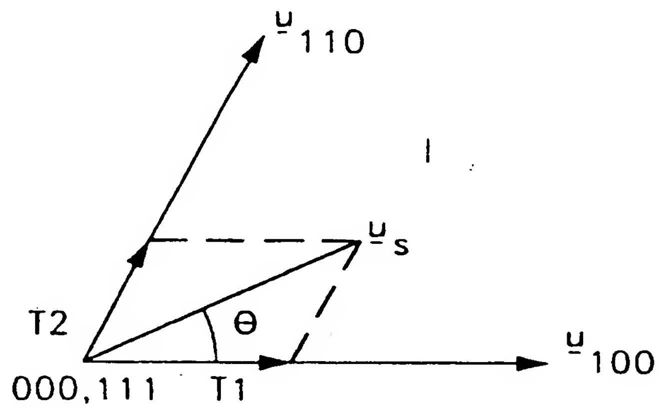


Fig. 3

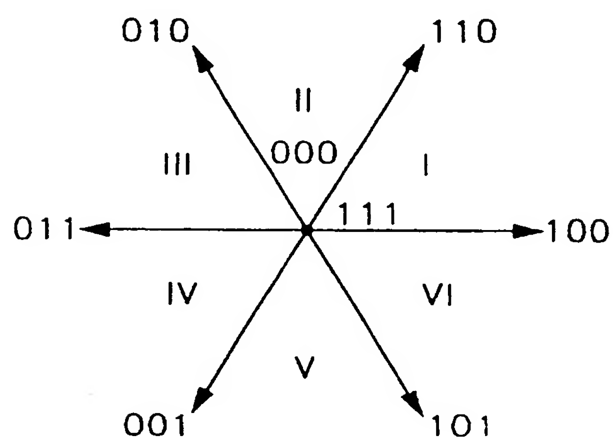


Fig. 4

Voltage Vector	DC-link current i_{DC}
$U_S=(100)$	$+i_{s1}$
$U_S=(110)$	$-i_{s3}$
$U_S=(010)$	$+i_{s2}$
$U_S=(011)$	$-i_{s1}$
$U_S=(001)$	$+i_{s3}$
$U_S=(101)$	$-i_{s2}$
$U_S=(000)=(111)$	0

Fig. 5

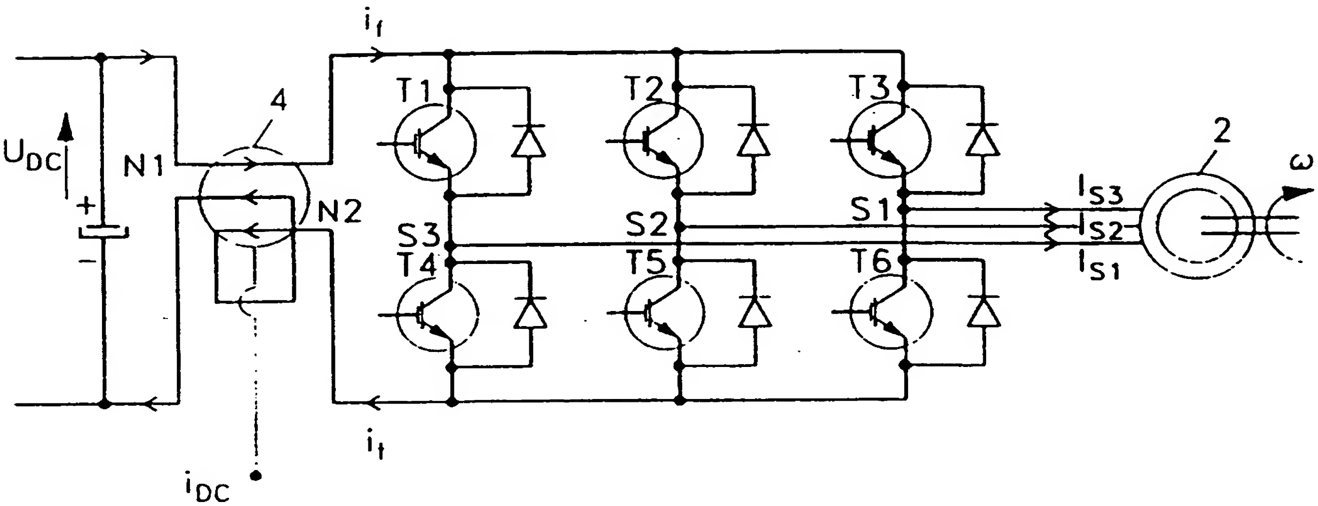


Fig. 6

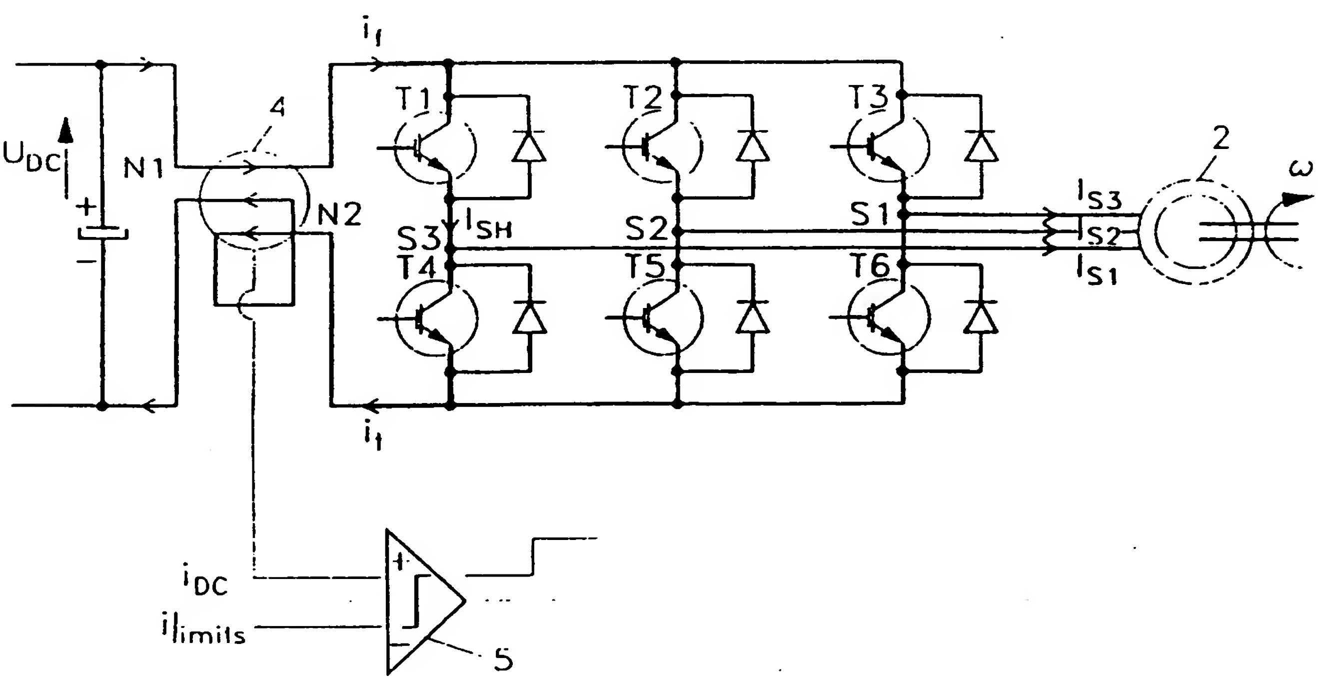


Fig. 7

BEST AVAILABLE COPY

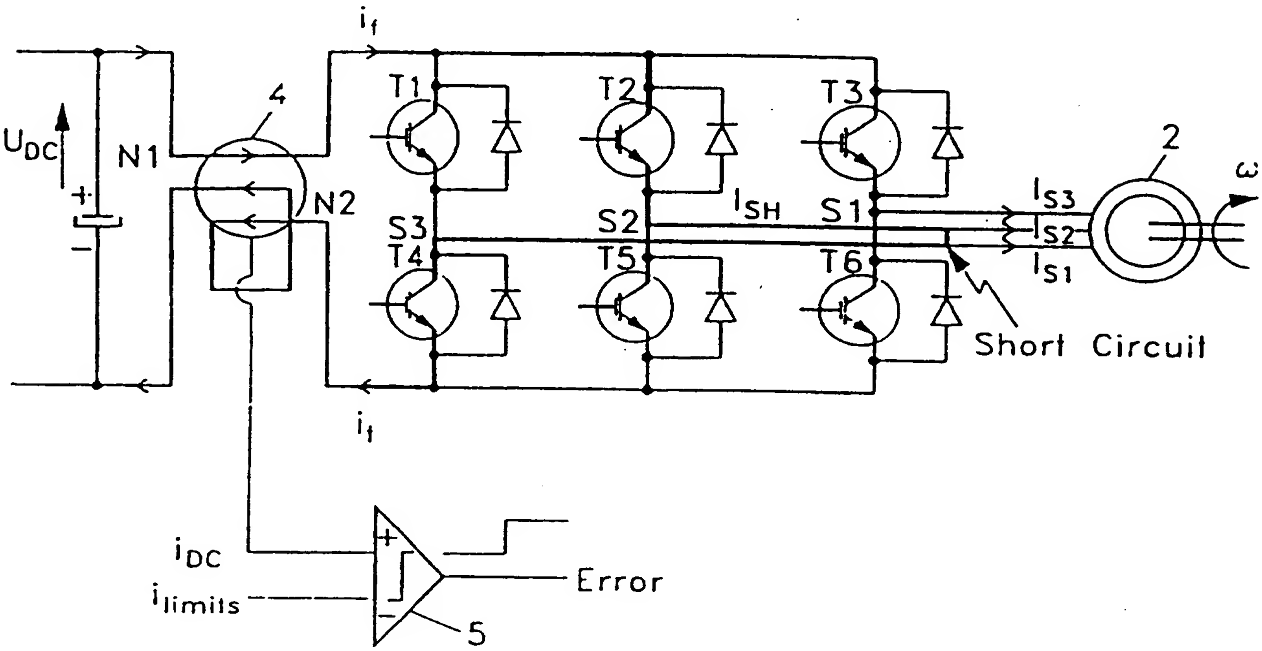


Fig. 8

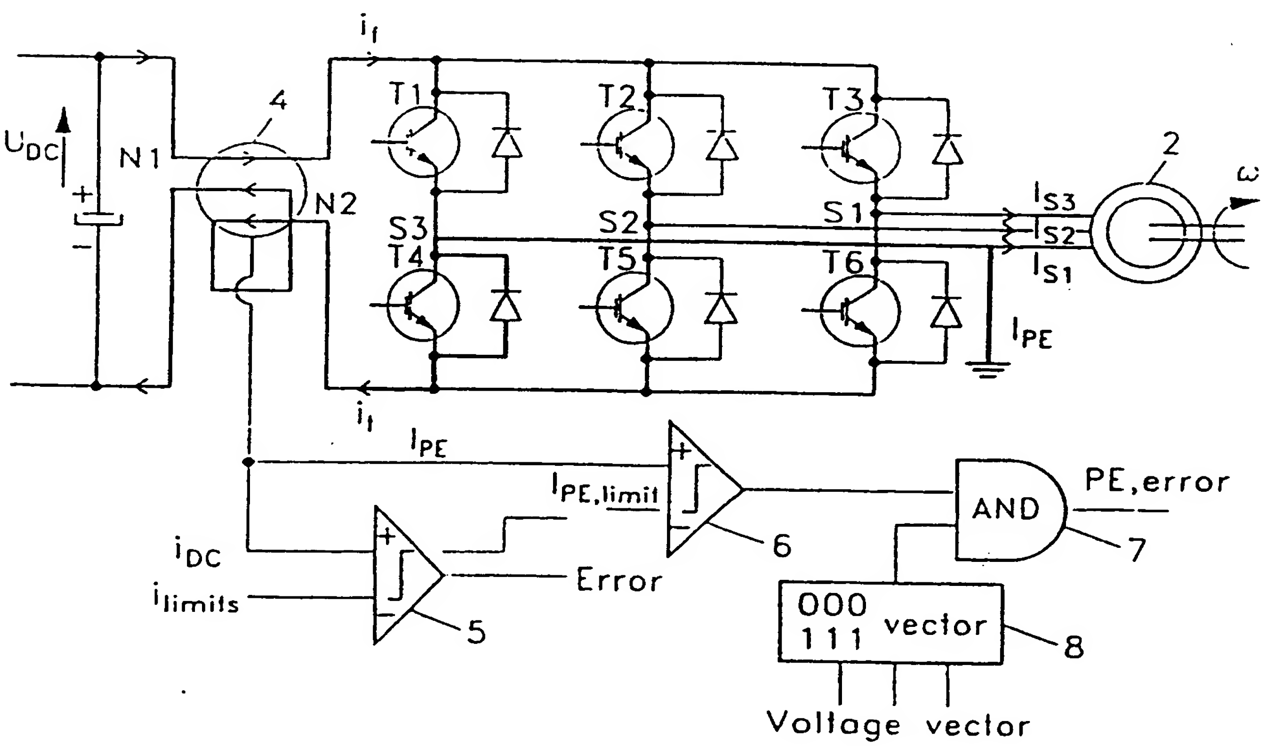


Fig. 9

BEST AVAILABLE COPY

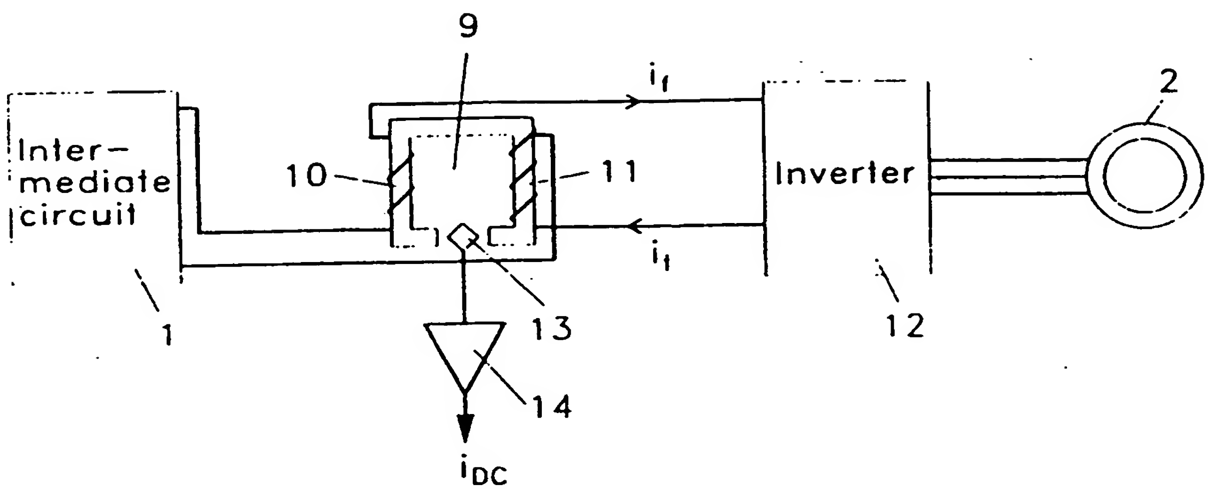


Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 96/00418

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H02H 7/122
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H02H, H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 4128961 C1 (LICENTIA PATENT-VERWALTUNGS-GMBH), 13 August 1992 (13.08.92), column 3, line 35 - column 5, line 3, figures 1-4	1-15
	--	
A	US 3760258 A (M. PERCORINI ET AL.), 18 Sept 1973 (18.09.73), column 2, line 38 - column 5, line 62, figures 1,2,4	1-15
	--	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" ertier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 February 1997	19 -02- 1997
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. + 46 8 666 02 86	Authorized officer Bertil Nordenberg Telephone No. + 46 8 782 25 00

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/DK 96/00418

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-C1- 4128961	13/08/92	NONE	
US-A- 3760258	18/09/73	AT-B- 327324	26/01/76
		BE-A- 793379	27/06/73
		CH-A- 563684	30/06/75
		DE-A,C- 2238809	05/07/73
		FR-A,B- 2166116	10/08/73